CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. (Original) A method of responding to a thermal trip signal from a processor in a computing system having multiple nodes, each node having one or more processors, comprising the steps of:

connecting a temperature monitor such that it may receive a thermal trip signal from each processor;

connecting a voltage control module to each node, the voltage control module operable to deliver voltage to all processors of the associated node when an enable signal is on and to shut off power to all processors of the node when the enable signal is off;

using the temperature monitor to: receive a thermal trip signal from an overheated processor; turn off the enable signal to the voltage control module of the node containing the overheated processor, such that the enable signal remains off during a system reset; and deliver a system power signal to a system reset controller; and

resetting the system, such that all nodes other than the node containing the overheated processor regain power.

2. (Original) The method of Claim 1, wherein the temperature monitor is a programmable logic device.

3. (Original) The method of Claim 1, wherein the thermal trip signal is a THERMTRIP signal.

4. (Original) The method of Claim 1, wherein the resetting step is performed by a system control unit.

5. (Original) The method of Claim 1, wherein the delivering step identifies the overheated processor.

6. (Original) The method of Claim 1, wherein the resetting step is performed automatically in response to the system power signal.

7. (Original) A temperature monitor for a computing system having multiple nodes, each node having one or more processors, and the computing system further responsive to a reset signal, the temperature monitor comprising:

logic circuitry operable to turn on or off an enable signal that determines whether all processors of a node receive power;

wherein the logic circuitry is further operable to receive a thermal trip signal from an overheated processor, to turn off the enable signal associated with the node containing the overheated processor, such that the enable signal remains off during a system reset, and to trigger a reset of the computing system.

8. (Original) The temperature monitor of Claim 7, wherein the temperature monitor is implemented with a programmable logic device.

9. (Original) The temperature monitor of Claim 7, wherein the temperature monitor turns on or off the enable signal via a connection to a voltage control module.

10. (Original) The temperature monitor of Claim 7, wherein the temperature monitor triggers the reset by delivering a signal to a system control unit.

11. (Original) The temperature monitor of Claim 7, wherein the temperature monitor is further operable to deliver a signal identifying the overheated processor.

12. (Original) The temperature monitor of Claim 7, wherein the temperature monitor is further operable to deliver a signal identifying the node of the overheated processor.

13. (Original) The temperature monitor of Claim 7, wherein the temperature monitor is further operable to respond to a PROCHOT signal.

14. (Original) An improved information handling system having multiple nodes, each node having one or more processors, and the computing system further responsive to a reset signal, the improvement comprising:

a temperature monitor operable to turn on or off an enable signal that determines whether all processors of a node receive power;

wherein the temperature monitor is further operable to receive a thermal trip signal from an overheated processor, to turn off the enable signal associated with the node containing the overheated processor, such that the enable signal remains off during a system reset, and to trigger a reset of the computing system.

15. (Original) The system of Claim 14, wherein the temperature monitor is implemented with logic circuitry.

16. (Original) The system of Claim 14, wherein the temperature monitor is implemented with a programmable logic device.

17. (Original) The system of Claim 7, wherein the system has a voltage control module and the temperature monitor turns on or off the enable signal via a connection to the voltage control module.

18. (Original) The system of Claim 14, wherein the temperature monitor triggers the reset by delivering a signal to a system control unit.

19. (Original) The system of Claim 14, wherein the temperature monitor is further operable to deliver a signal identifying the overheated processor.

20. (Original) The system of Claim 14, wherein the temperature module is further operable to respond to a PROCHOT signal.